REMARKS

Applicants thank the Examiner for the very thorough consideration given the present application.

Claims 1-24 are now present in this application. Claims 1, 9, 16 and 20 are independent.

Claims 1-9, 11, 13-16 and 19-23 have been amended. Reconsideration of this application, as amended, is respectfully requested.

Drawings

Applicants have not received a Notice of Draftsperson's Patent Drawing Review PTO-948 or other indication of whether or not the drawings have been approved by the Draftsperson. Since no objection has been received, Applicants assume that the drawings are acceptable and that no further action is necessary. Confirmation thereof in the next Office Action is respectfully requested.

Claim Objections

The Examiner has objected to claims 6, 7, 8, 14 and 15 because of several informalities. In order to overcome this objection, Applicants have amended claims 6, 7, 8, 14 and 15 in order to correct the deficiencies pointed

out by the Examiner. Reconsideration and withdrawal of this objection are respectfully requested.

Rejection Under 35 U.S.C. § 102

Claims 1-15 and 20-24 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,658,579 to Bell et al. (Bell). This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

While not conceding the appropriateness of the Examiner's rejection, but merely to advance prosecution of the instant application, Applicants respectfully submit that independent claim 1 has been amended to recite a combination of elements in a local timing circuit for direct use with transport logic in a network element, including selecting a selected timing signal and *distributing the selected timing signal directly to the transport logic*. Applicants respectfully submit that this combination of elements as set forth in independent claim 1 is not disclosed or made obvious by the prior art of record, including Bell. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

The Examiner states that external controller cards 542b and 543b include external central timing subsystems, for example EX CTS 750. In the Background of the Invention, Bell provides that "it is crucial" that components and cards

within the network device transfer data according to the same synchronized timing signals, as transferring data at different times, even slightly different times, may lead to data corruption, the wrong data being sent and/or a network device crash. Distributing clock signals, therefore, must be done carefully to insure that the clock signal received by each component is not skewed with respect to the clock signals received by other components (see Bell, Col.1, lines 35-43). In other words, Bell seeks to synchronize all clock signals to one source.

The Applicants' respectfully submit that the external central timing subsystems (EX CTS) of Bell operate in practically the same manner as the systems of the Applicants' disclosed background art. For example, in Bell, the timing signal(s) generated by the plurality of EX CTS 750s are delivered to local (EX LTS) timing subsystems for synchronization, and in turn, the local timing subsystems distribute a selected timing signal to the transport logic. Therefore, the controllers of Bell that employ the centralized EX CTS 750s have the same disadvantages as the Applicants' disclosed background art. Particularly, the central timing subsystems EXT CTS 750s do not distribute a selected timing signal directly to the transport logic. Rather, as in the Applicants' disclosed background art, the result of using the centralized timing systems EX CTS 750s of Bell is that all line cards must synchronize to their respective data using timing signals generated from one timing source.

An illustration of the signal distributions from the centralized (EX CTS 750) to local timing subsystems (EX LTS 756) is provided in Fig. 49 of Bell. In other words, the signal distributions are from central-to-local as opposed to local–to-local. In contrast, in the Applicants' claimed invention, the need for the centralized timing subsystem is eliminated.

Fig. 50C of Bell shows the output of the EX CTS 750 e.g., STRAT_REF1 . . . STRAT_REF18, which are provided to EX LTS 756 and also to other EXT CTS 750s. Particularly, Bell provides that "STRAT_FB 754 is an external timing reference signal from the EX CTS (one of STRAT_REF1-STRAT_REFN) that is routed onto the mid-plane(s) and back onto the local printed circuit board such that is most closely resembles the external timing reference signals sent to the EX LTSs and the other EX CTS "in order to minimize skew" (see Bell, Col.78, lines 27-30).

The above-mentioned "skew" is a major concern in Bell. As a solution to the skew problem, Bell provides multiple EX CTSs for distributing the timing reference signals to the local timing subsystems. This approach is in addition to the basic scheme disclosed in the Applicants' background art (one CTS per multiple LTSs). For example, Bell provides as follows:

> Since timing is so critical to network device operation, typical network devices include redundant central timing subsystems. Certainly, the additional reference timing signals from a redundant central timing subsystem to each of the forwarding cards and switch fabric cards create further routing difficulties. In addition, if

> the two central timing subsystems (i.e., sources) are not synchronous with matched distribution etches, then all of the loads (i.e., LTSs) must use the same reference clock source to avoid introducing clock skew--that is, unless both sources are synchronous and have matched distribution networks, the reference timing signals from both sources are likely to be skewed with respect to each other and, thus, all loads must use the same source/reference timing signal or be skewed with respect to each other.
>
> Bell, Col.64, lines 12-27

Applicant notes that the LTSs (local timing subsystems) in the above-recited portion of Bell are referred to as the "load". Such a reference provides further confirmation that a timing reference signal is distributed to the LTS (the load) and not directly to the transport logic.

For the reasons set forth above, Bell fails to teach the combination of elements recited in independent claim 1 (as amended).

Claim 9 has been amended to recite a combination of elements in a *decentralized* synchronization system for use in a network element, including *two or more local determination circuits located on the two or more local circuit assemblies which are directly coupled together via a communicationchannel*.

Claim 20 has been similarly amended to recite a combination of steps in method for synchronizing transport logic in a network element including determining that a selected local circuit assembly *among said two or more local circuit assemblies which are directly coupled together via a communication channel* is a master circuit assembly and that remaining circuit assemblies are

slave circuit assemblies.

Bell, argued above with respect to independent claim 1, does not teach the recited claim combinations in a decentralized or local timing subsystem. In this regard, Bell fails to teach or suggest the combinations of elements recited in independent claims 9 and 20 (as amended). In other words, the timing system referenced by the Examiner is a centralized timing system (as in the background art), and therefore does not meet the Applicants' claimed decentralized or local timing circuits. This alone makes the rejection under 35 U.S.C. 102 improper.

Still further, with respect to independent claim 9, Bell fails to teach the Applicants' claimed feature *communication channel directly coupling* at least a pair of local circuit assemblies. Similarly, with respect to independent claim 20, Bell fails to teach two or more local circuit assemblies that are *directly coupled together via a communication channel*.

Particularly, Bell teaches two mid-plane circuit boards 622a and 622b (see Bell, Fig. 41c). The mid-plane circuit boards of Bell (asserted communication channel) are each connected to dozens of cards (see Bell, Col. 58, lines 45-48). Bell further provides that through each mid-plane, the cross-connection cards in each quadrant may transfer network packets between any of the universal port cards in its quadrant and any of the forwarding cards in its quadrants. However, in the mid-plane circuit boards of Bell,

communications between cards is not through a direct card-to-card coupling arrangement. Rather, communication is accomplished through a switching scheme managed by the switch fabric cards (see Bell, Col. 59, lines 1-6). In other words, Bell does not teach direct coupling between cards via a communication channel.

For the reasons set forth above, Bell fails to teach the above-recited features of independent claims 9 and 20. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

With regard to dependent claims 2-8 and 10-15, Applicants submit that claims 2-8 and 10-15 depend, either directly or indirectly, from independent claims 1 and 9, which are allowable for the reasons set forth above, and therefore claims 2-8 and 10-15 are allowable based on their dependence from claims 1 and 9. Reconsideration and allowance thereof are respectfully requested.

Rejections under 35 U.S.C. §103

Claims 16-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Bell in view of U.S. Patent No. 6,317,439 to Cardona. This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

While not conceding the appropriateness of the Examiner's rejection, but merely to advance prosecution of the present Application, Applicants respectfully submit that independent claim 16 has been amended to recite a combination of elements in a synchronization system for use with an add/drop multiplexer card set in a network element including, a communication channel *directly coupling a card in said add/drop multiplexer card set to another card in said add/drop multiplexer card set*. Applicants respectfully submit that the combination of elements as set forth in independent claim 16 is not disclosed or made obvious by the prior art of record, including Bell and Cardona.

Bell, argued above with respect to independent claims 9 and 20, fails to teach a communication channel directly coupling circuits. In making this rejection, the Examiner asserts that mid-plane 622a meets the communication channel of the Applicants' claimed invention. However, as set forth above, mid-plane 622a provides connections for many cards or circuits, but none directly. The mid-plane 622a is a switching network (not a channel). Therefore, as in the case of independent claims 9 and 20, Bell fails to teach the above-recited features of independent claim 16, as amended. Cardona cannot supply the deficiency of Bell. Reconsideration and withdrawal of this art grounds of rejection are respectfully requested.

With regard to dependent claims 17-19, Applicants submit that claims 17-19 depend, either directly or indirectly, from independent claim 16, which is

allowable for the reasons set forth above, and therefore claims 17-19 are allowable based on their dependence from claim 16. Reconsideration and allowance thereof are respectfully requested.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone Percy L. Square, Registration No. 51,084, at (703) 205-8034, in the Washington, D.C. area.

Prompt and favorable consideration of this Amendment is respectfully requested.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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